Filing Date: December 21, 2000

Title: METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT USING A DUAL POLY PROCESS

#### **REMARKS**

This responds to the Office Action mailed on September 28, 2004.

Claim 42 is amended, and no claims are canceled or are added; as a result, claims 38–45, 47–65 and 68–75 remain now pending in this application.

# §102 Rejection of the Claims

Claims 38-45, 47, 53-56, 58, 60-62, 64, and 68 were rejected under 35 USC § 102(e) as being anticipated by Applicants' Assignee's (Micron Technology, Inc.'s) U.S. Patent 5,506,172 which was issued April 9, 1996 to Sanh Tang, who is one of the two named co-inventors of the present application. Applicants respectfully traverse the rejection and request that the claims be reconsidered and allowed in view of the following remarks.

The Office Action contends that Figures 1–13 of the Tang patent are where "Tang teaches the claimed process<sup>1</sup>." More specifically, the Office Action contends<sup>2</sup> that Tang FIG. 9 teaches the claim feature – "...a first polycrystalline silicon layer overlying the oxide region but not the first substrate region having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide region..<sup>3</sup>" In countering the position taken by Applicants in the previous Response, the Office Action states: "It appears that Applicants are relying on the features of oxide 44, whereas the Examiner is relying on polysilicon 48/66 where the lower part of the polysilicon is above oxide layer 46<sup>4</sup>." Applicants respectfully traverse that assertion as set forth below.

The above quoted assertion rests upon an implied assertion that oxide 44 and oxide layer 46 of Tang are different layers. Such is not the case. FIG. 6 of Tang shows that the field oxide 44 and associated gate oxide 46 comprise a single oxide region formed of a single layer of material. In the language of the claim, the oxide region is "overlying at least a portion of the second substrate region" so that the first substrate region is that portion of the substrate layer which has no overlying oxide region – i.e. the contact opening 52. In applying Tang FIG. 9 to

Office Action, page 4, line 7, Paragraph 4

<sup>&</sup>lt;sup>2</sup> Office Action, page 2, line 2 of final paragraph

<sup>&</sup>lt;sup>3</sup> Office Action page 2, lines 8–10.

<sup>&</sup>lt;sup>4</sup> Office Action, page 2, lines 2-5 of final paragraph.

Serial Number: 09/745,780

Filing Date: December 21, 2000

METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT USING A DUAL POLY PROCESS Title:

Dkt: 303.451US6

the claim, the Office Action treats conductive line portion 66 of first conductive layer 48 as the "first polycrystalline silicon layer" of the claim. If one then looks to the thickness of that first polycrystalline layer it can be seen that its lowest upper surface - the one marked in FIG. 9 as "outermost surface 70" - is actually *lower* than the "highest upper surface" of the claimed "oxide region" designated by reference characters 44/46. When Tang is properly construed, the highest upper surface of the oxide region 44/46 is the upper surface of the field oxide 44 portion of the oxide region 48/46. Applicants contend that the Office Action's treating of the gate oxide portion 46 as somehow separate from field oxide portion 44 is an artificial and unrealistic reading of the claim language and of Tang. Because Tang does not show the disputed feature of claim 38, it cannot support an anticipation rejection of that claim. Nor can Tang be a proper anticipation reference against claims 39-45 and 47-52 which incorporate a similar limitation or dependent claims 53-65 and 68-79 which include the limitation as well as other features.

Reconsideration and allowance of the pending claims is respectfully requested.

## **Double Patenting Rejection**

Claims 38-45, 47-65, and 68-70 were rejected under the judicially created doctrine of double patenting over claims 1-40 of U.S. Patent No. 6,659,632.

Applicants do not admit that any claims herein are obvious in view of Patent No. 6,659,632. Applicants' Assignee, on information and belief does not own that patent. Withdrawal or correction of the improper double patenting rejection is respectfully requested. If a corrected rejection is to be made, it is respectfully submitted that it should be in a non-final rejection.

### Interview summary

The Examiner's summary of the November 29 telephone conference with the undersigned is believed to be correct. The present Final Rejection responded to remarks made in Applicants' July 6, 2004 Response that were not dealt with in the prior Final Office Action.

Page 14 Dkt: 303.451US6

#### AMENDMENT AND RESPONSE UNDER 37 CFR § 1.116 – EXPEDITED PROCEDURE

Serial Number: 09/745,780

Filing Date: December 21, 2000

Title: METHOD FOR FORMING AN INTEGRATED CIRCUIT INTERCONNECT USING A DUAL POLY PROCESS

### **CONCLUSION**

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6970 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

MARTIN C. ROBERTS ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 373-6970

Date Jet many 16, 2005

Charles E. Steffey

Reg. No. 25,179

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this \_\_\_\_\_\_ day of February, 2005.

Ting Kahart

Signature

Name